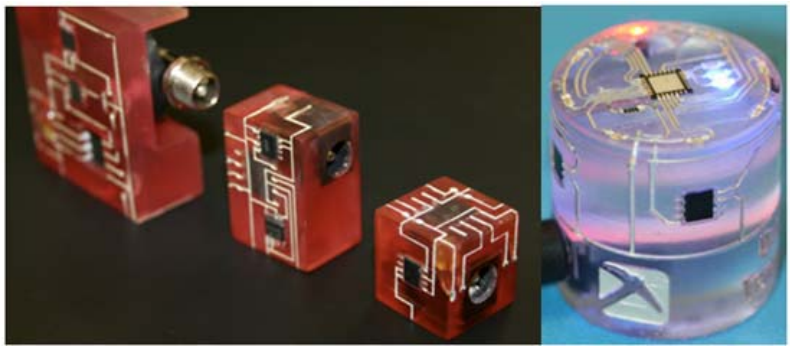
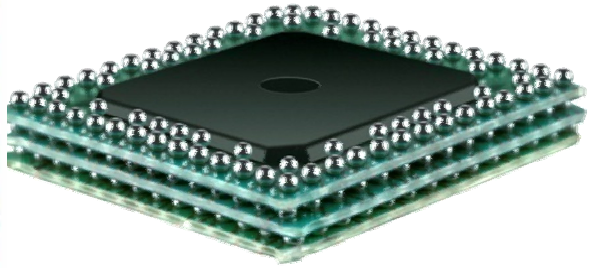
IDEA – "Innovations & Developments in Electronics Assembly"





State-of-the-Art Technology Workshops 2015

WS 1 – 3D PRINTED ELECTRONICS, NANO COATINGS AND VITAL TECHNOLOGY TRENDS IMPACTING ELECTRONICS ASSEMBLY – ENVISION THE FUTURE FOR SUCCESS (1 ½ day)

WS 2 – PROCESS DEVELOPMENT AND YIELD ENHANCEMENT INVOLVING ADVANCED PACKAGES, 01005 and PoP ASSEMBLY (2 Days)

WS 3 – BASIC SMT: FUNDAMENTALS OF SMT PROCESSES (1 Day)

WS 4 – SMT FOR THE PACKAGING, BACKEND & PCB PROFESSIONALS (2 Days)

WS 5 – BGAs & CSPs: SOLUTION ORIENTED SMT MANUFACTURING TECHNIQUES FOR ENHANCED ASSEMBLY & YIELD (2 Days)

WS 6 – BRIDGING THE GAP FROM CHIP TO BOARD – LEVERAGING COB TECHNOLOGY IN SMT & PACKAGING APPLICATIONS

WS 7– IMPLEMENTING FLIP CHIP ASSEMBLY IN MAINSTREAM SMT & PACKAGING APPLICATIONS (1 Day)

WS 8 – SOLDERING METALLURGY: SCIENCE & PRACTICE IN SMT PROCESSES (1 Day)

WS 9 – TIN WHISKERS: RISK ASSESSMENT & MITIGATION STRATEGIES (1 Day)

3D PRINTED ELECTRONICS, NANO COATINGS & VITAL TECHNOLOGY TRENDS IMPACTING ELECTRONICS ASSEMBLY – ENVISION THE FUTURE FOR SUCCESS"

WS1 – 1 ½ Day

OVERVIEW

Electronics packaging and assembly is being revolutionized by creative bold new ideas challenging boundaries of conservative thinking. Take for instance 3D printing. 3D printers and 3D printing services have proliferated. 3D Printed Electronics as the next phase is already on its way – no longer a novelty but commercial reality. Going 3D eliminates conventional PCB design constraints on the layout of components and inefficiencies on space and material. The implications are stunning - the PCB can take any conceivable shape, no longer just planer. Printing of electronic components is another spin off. On another innovative front Nano-coating technology is finding promising applications as fluxo-phobic coatings on stencils for solder paste printing. Similar shifts in thinking are visible in other areas: Cleaning of PCBAs is resurging to improve reliability; long Term reliability threats such a Conductive Anodic Filaments (CAF), Creep Corrosion, Pad Cratering, are gaining the focus of industry and researchers. With increased understanding of the interactive variables measures are evolving to mitigate their impacts. Embedded passives, another innovative area, like the case of 3D printing, offers opportunities transforming the way the industry perceives PCB assembly.

This workshop provides knowledge and insights on above challenges and innovative technology fast translating into today's reality.

"History shows that Leading Edge Organizations succeed by adapting to innovative change, while others, like the Titanic, steam blindly into the future"

WORKSHOP COVERAGE

This workshop focuses on Innovative Technology Trends, emerging new issues and assembly process transforming Electronics Packaging and SMT. It starts by reviewing the captivating field of 3D printing, its evolution, 3D technologies, combining 3D with Electronics, applications such as MIDs, industry products and future. Leading innovations includes Nano-Coatings on stencils, their evolution, composition, operating principles and application methods. The section includes industry comparisons quantifying the results on solder paste printing with different materials and fluxes. Issues such as Conductive Anodic Filaments (CAF) failures occurring subsurface of the PCB are examined - definition, causes, progression, identification testing and differences from surface electromigration; it's impacts and prevention strategies are examined. Other reliability issues such as Creep corrosion, Pad Cratering, Tin Whiskers and latent ESD Damage are addressed together with prevalent industry mitigation practices. Leading edge process areas include PCBA cleaning, plasma etching, conformal coatings and - materials, equipment and processes. Packaging trends covers the fast transforming field of Packaging and driving factors leading to 2.5D and 3D approaches and implications to both SMT and Packaging segments. A major highlight of the program is in depth coverage of the latest Lead free finishes, their properties, metallurgy, compatibility and associated standards. A bonus module provides knowledge into to field of Embedded Passives. Videos and highly graphical content is embedded to enhance the learning experience. The content is enriched by references and review of different industry studies. Reference materials are provided in a CD ROM to the participants for further learning. A unique feature of our workshops is pre and post event technical support by phone or email to all participants.

AUDIENCE

This is a high level program designed to meet the requests on topics of interest expressed by leading edge SMT professionals eager to stay ahead. It will greatly benefit Engineering, Process Planning and Development, Failure Analysis, and 'industry watch' personnel.

3D PRINTED ELECTRONICS, NANO COATINGS & VITAL TECHNOLOGY TRENDS IMPACTING ELECTRONICS ASSEMBLY – ENVISION THE FUTURE FOR SUCCESS"

WS1 – 1 ½ Day

WORKSHOP AGENDA

MODULE 1 – INTRODUCTION TO 3D PRINTED ELECTRONICS

- Scope and Overview of 3D Creation
- Base 3D Technology
  - FDM (Fuse Deposition Modeling)
  - FFF (Fuse Filament Fabrication)
  - LDS (Laser Direct Structuring)
  - MJM (Multi Jet Modeling)
  - SLA (Stereo Lithography)
  - Other 3D Technologies
- Combining 3D & Printed Electronics
  - Conductive Materials
  - Conductive Track Deposition
  - Masking Materials
  - Process steps example
- MID (Molded Interconnect Devices)
- From Soft Ware to Physical reality
- Applications – Prototyping, Small Batch Manufacturing, Automotive, Industrial, Medical & Multi-functional Parts
- 3D Organizations, Products and Technology Matrix
- Summary and Future work

MODULE 2 – NANO COATINGS FOR STENCIL PRINTING OF SOLDER PASTE

- Nano Coatings Overview & Evolution
- Types of Coatings
- Coating Properties
- Compatibility with Materials
- Print Parameters Study Matrix
- Comparison of Different Results Data
- Application Methods & Costs
- Answers to FAQs

MODULE 3 – PCB RELIABILITY ISSUES

Conductive Anodic Filaments

- Subsurface Electromigration vs. Dendrites
- Current Theories of CAF
- Failure Modalities
- Limitations of SIR
- Variables impacting CAF
  - Resin systems
  - Finishing
  - Drill metals residuals
  - Bias
  - Fluxes
  - Environmental
- Recommendations

Creep Corrosion

- What Is It and Causes
- Appearance Examples
- How it Differs from Electro Migration
- Impact – How, Where and who
- Mitigation Practices
- Design Recommendations

PCB Pad Cratering

- What It is and its Causes
- How Serious and Why It Impacts
- Assessment Methods
- Findings and Recommendations

Tin Whiskers

- Impacts
- Cause Hypothesis
- Assessing Risk
- Current Mitigation Practices

Latent ESD Damage

- Manifestation
- How it Differs
- Appearance
- Impacts
- Control

MODULE 4 – INTERCONNECTION TRENDS

- Packaging Evolution
- Approaches Towards Higher Levels of Integration
- 3D with and without TSV
- Die and Package Stacking
- Applications and Examples

MODULE 5 – PROCESS TRENDS

Plasma Stripping and Cleaning

- Principles and Application Scope
- PCBA Cleaning
- Stripping & Etching Applications
- Equipment & Configuration
- Measuring and Improving Cleaning Efficacy

Conformal Coatings

- Science and Application
- Material properties and selection
- Process and Equipment Set-up
- Test standards

MODULE 6 – LATEST LEAD FREE FINISHES

Metallurgy, Comparison, Issues, Compatibility and Applicable Standards for:

- ENEPIG
- DIG
- Selective ENIG OSP
- ENIG
- I Ag
- I Sn
- EPNi and ENi
- OSP
- LF HAL

MODULE 7 – EMBEDDED PASSIVES

- Function & Scope
- Process Options
- Types of Material Used & Available
- Impacts – Limitations & Cost

MODULE 8 – CONCLUSION

- Summary
- Reference Materials

PROCESS DEVELOPMENT AND YIELD ENHANCEMENT INVOLVING ADVANCED PACKAGES, 01005 and PoP ASSEMBLY

WS2 – 2 Days

COVERAGE

This workshop provides a comprehensive coverage of advanced assembly techniques, materials and processes involved in state-of-the-art SMT assembly. It is designed to gear both the SMT and the packaging professional to understand most current SMT trends and practices and to resolve process issues. It provides knowledge on control and management of process, yield, and the tools and techniques for failure analysis and process development.

Upon completion of this workshop, the participants will be able to improve yields, reduce assembly defects and gain a confident foothold into process development techniques as well as acquire the specialized knowledge and considerations for usage in their respective field.

WORKSHOP AGENDA

MODULE 1 – ASSEMBLY OVERVIEW
- SMT Assembly & Package Trends
- Product & Process Driving Factors
- From Mainstream to Direct Chip Attachment
- SiPs, MCMs & 3-D Applications
- Yield & Process Capability Needs

MODULE 2 – PROCESS CONSIDERATIONS
- Interactive Variables
- Solder Paste Considerations
- 0201 / 01005 & Small Form Factor Devices
- The Importance of Solder Volume Calculations
- Solder Volume For Odd Form Devices – Spreadsheet Example
- Solder Volume Process Window
- Solder Paste Release
- Pad Design & Layout
- Solder Volume & Pad Designs for BGAs
- Practical Tips, Guidelines & Control

MODULE 3 – POP / PIP ASSEMBLY
- Understanding PoP / PiP
- Structures and Variants
- Approach and Comparisons
- Associated Standards
- PoP / PiP Assembly
- PoP / PiP Process Options, Helpful Tips and Guidelines

MODULE 4 – REFLOW ENGINEERING
- High Yield Considerations
- Understanding & Managing Heat Transfer
- Understanding Reflow Ovens & Technology
- Thermal Profiling Considerations
- Profiling for BGAs
- Reflow Process Window
- Moisture Sensitivity of Devices - IPC/Jedec Standard

MODULE 5 – METALLURGY & MATERIALS
- Types of Alloys
- Intermetallic Compounds – Binary, Ternary
- Metallization Considerations – Gold, Silver, Tin & Nickel
- Lead Free Vs. Sn/Pb Alloys – Impacts

MODULE 6 – ADDRESSING PROCESS ISSUES
- Solder Balling
- Tombstoning – Maths & Science
  - Root Cause
  - Different Signatures
  - Impact of Solder Volume
  - Other Interactive Variables
- Bridging & Opens
- Non-Wetting
- 'Black Pad' Issues
- Solder Migration
- Voids
- Low Shear Strength Failures
- Fillet Lifting
- Tin Whiskers

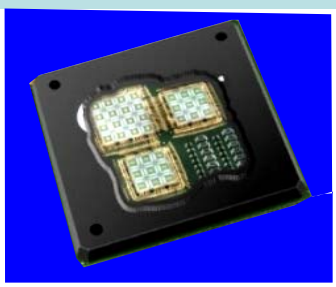
MODULE 7 – ANALYTICAL TOOLS & TECHNIQUES
- Equipment Classification, Types & Principle Function
- Microscopy & Imaging – SEM, SAM, RI
- Surface & Metallization – Scanning Probe, AFM, MI
- Materials Behavior – TMA, MI, DSC
- Contamination Analysis – FTIR
- Analytical Equipment – SMT Application Chart

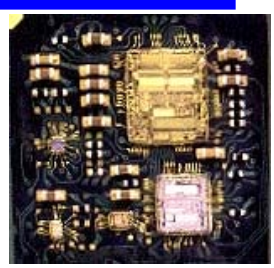
MODULE 8 – CONFORMAL COATINGS
- Definitions
- Coating Options
- Advantages
- Process Options and Comparisons
- Setting up the Spray Facility
- Safety Concerns

MODULE 9 – CONCLUSION
- Appendix & Glossary
- References
- Listing of Applicable Standards
- Solder Volume Calculation Spread Sheet

OVERVIEW

The goal of greater functional integration is impacting both SMT assembly and IC Packaging with technological challenges. Numerous package styles, multi-chip packages and 3D Packaging approaches are changing the face of traditional SMT assembly. The growth of packages involving multiple dies on organic substrates has brought SMT processes into the realm of the Packaging industry. SMT know-how is being rapidly adopted by the backend process in the manufacturing of MCMs, SiPs, custom packages and specialty modules. Both the SMT and the packaging professionals face the vital need to acquire concepts and know-how geared towards their environment. This demands understanding leading edge processes, configurations, metallurgy and material sciences for successful implementation. As traditional SMT assembly and Packaging rapidly head towards the common goal of greater functional integration, there is vital need for organizations to acquire new knowledge, understand the assembly processes, the issues and considerations - indeed it is a vital step towards success.





AUDIENCE

Engineering personnel from Manufacturing, Assembly, Equipment, Materials, Maintenance and Failure Analysis disciplines. Technicians or Supervisory levels with adequate grasp of SMT concepts and experience will also benefit and gain applied knowledge. Target industries include PCB assembly, EMS/ESPs and those segments of IC packaging incorporating SMT concepts and/or requiring skills to address their end-user product utilization and processing issues.

BASIC SMT – FUNDAMENTALS OF SMT PROCESSES

WS3 – 1 Day

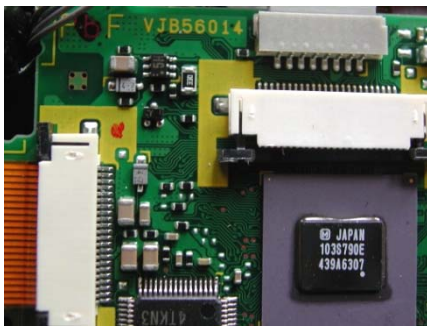
COVERAGE

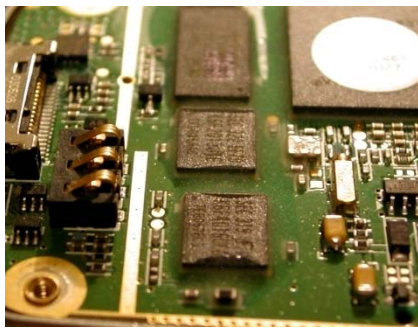
Through this course the participants will be able to:

a) Understand terminologies used in SMT, measurement and communication.
b) Acquire knowledge of SMT materials, equipment and interactive variables.
c) Understand SMT inspection and address common process issues.

OVERVIEW

This is a basic through intermediate level SMT workshop for the relatively newcomer to the SMT field with modest experience. The course provides an overview of the technicalities of the SMT Process. This course will fast track participants to acquire a formal and objective understanding of the technology.





WORKSHOP AGENDA

MODULE 1 – SMT CONCEPTS

- SMT Component Evolution
- Types of SMT Processes

MODULE 2 – SOLDER PASTE, PRINTING & DEPOSITION

- Variables Fishbone
- Solder Paste Composition & Characteristics
- Fluxes: RMA, WS, No-clean, Low Residue
- Solder Paste Qualification & Control
- Stencil Engineering
- Substrates & Squeegees Control Aspects
- Printing Process Control & Optimization
- Trouble-shooting Solder Paste Printing
- Auditing The Printing Process

MODULE 3 – PICK AND PLACE

- Categorization of Placement Equipment
- Placement Throughput
- Placement Accuracy
- Practical Tips and Trouble-shooting:
- Misplacement, Rotation, Missing, Cracked or Damaged Components

MODULE 4 – REFLOW SOLDERING

- Variables Fish Bone
- Heating Modes & Impact
- Ovens and Importance of Maintenance
- Thermal Profiling Methods
- Linear Ramp Profiles

MODULE 5 – WAVE SOLDERING

- Fundamentals of Wave Soldering
- Fluxing Systems
- Wave Shapes and Dynamics
- Wave Soldering Variables
- Managing and Adjusting Wave Parameters
- Addressing Common Issues

MODULE 6 – SOLDER JOINT REQUIREMENTS

- Inspection Criterion
- Typical SMT Defects & Causes

MODULE 7 - REWORKING SMT BOARDS

- Rework Considerations - When, Where & How?
- Rework Equipment Options & Applications
- Two Terminal, Multi-Leaded & FPQFP Rework
- Helpful Tips

MODULE 8 – CONCLUSION

- Applicable Standards
- Useful Websites
- Reference Magazines & Journals
- Glossary of Printing Terms
- Glossary of SMT Terms & Acronyms
- Audit Checklist

AUDIENCE

SMT Engineering and Assembly Line Personnel, Process and Equipment Techs, Incoming, QA and materials

SMT FOR THE PACKAGING, BACKEND & PCB PROFESSIONALS

WS4 – 2 Days

COVERAGE

This workshop provides a comprehensive coverage of advanced technology, materials and process interactions involved in state-of-the-art Packaging and SMT PCB assembly. The workshop content is designed to benefit the Packaging / Backend engineer who wants to embark on a rapid SMT learning curve specific to their environment. It will also benefit the SMT professional to understand current SMT trends and practices. Particular emphasis is placed, for example on critical areas such as solder paste and printing, cleaning processes and impacts and the interactions of materials and processes on assembly yield. Participants learn how to practically address process issues for yield improvement and to enhance processes using failure analysis tools and techniques. Real life examples and findings from many of latest studies are incorporated to improve learning. Upon completion of this workshop participants will improve process yields, prevent assembly defects and gain a confident foothold into process development by acquiring the specialized knowledge and considerations applicable to their field.

OVERVIEW

The goal of greater functional integration is impacting both IC Packaging and SMT assembly with common technological challenges. The rapid growth and adoption of packages involving multiple dies on organic substrates has brought SMT processes into the Packaging industry. SMT know-how is being rapidly adopted by the backend process in the manufacturing of Multi-Chip-Modules (MCMs), Systems-in-a- Package (SiPs) and other custom packages and specialty modules. Like wise the mainstream SMT professional faces the challenges of assembling complex packages and to understand their special needs and process impacts. As the industry heads towards the common direction and goal of higher levels of functional integration both the Packaging and SMT professionals face the vital need to bridge the knowledge, understand the process issues, considerations and impacts in order to remain competitive in the evolving environment.

WORKSHOP AGENDA

MODULE 1 – SOLDER PASTE & FLUXES
- Process Interactive Variables
- Solder Paste Constituents
- Solder Powder & Fluxes
- Solder Paste Properties
- Solder Paste Qualification Testing & Standards
- Solder Paste Sensitivities
- Paste and Flux Impact on the Process

MODULE 2 – FLUX REMOVAL & CLEANING
- Cleaning Definition
- Types of Contaminants
- Cleaning Systems Principles
- Chemistry Options
- Cleaning Low Standoff Height Components
- Flux residue impact on Underfill
- Cleaning Measurements & Standards
- Discussion on Several Technical Papers

MODULE 3 – PASTE PRINTING & PROCESS
- 0201/ 01005 Small Form Factor Devices
- The Importance of Solder Volume
- Solder Volume For Odd Form Devices
- Solder Volume Process Window
- Solder Paste Release
- Stencil Technology
- Pad Design Guideline
- Solder Volume & Pad Designs for BGAs
- Stencil and Pad Design Yield Impact
- Practical Guidelines & Control

MODULE 4 – REFLOW ENGINEERING
- High Yield Considerations
- Understanding & Managing Heat Transfer
- Reflow Ovens Technology
- Oven Impact on Tombstoning
- Oven Maintenance & Micro Solder Balls

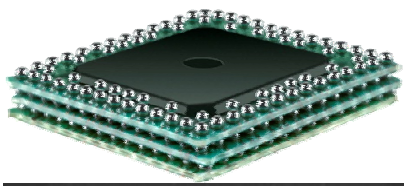
MODULE 5 - THERMAL PROFILING
- Profiling - Key Segments
- Linear vs. Ramp Profile
- Profiling Requirements Vs. Solder Paste/ Flux
- Understanding Thermocouples
- Techniques for Profiling Accuracy
- Profiling for BGAs
- Reflow Process Window & PWI
- Impact of Oven Loading
- Moisture Sensitivity of Devices - IPC/Jedec Stds.

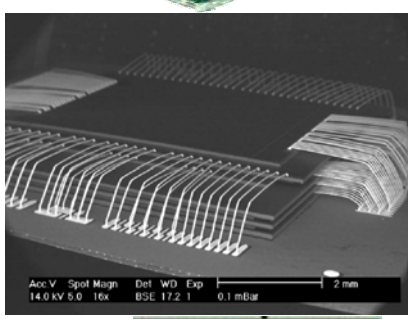
MODULE 6 – METALLURGY & MATERIALS
- Types of Alloys
- Equilibrium Phase Diagrams
- Intermetallic Compounds – Binary, Ternary
- Sn Metallurgical Interaction with –
- Cu, Au, Ag, & Ni
- Surface Finishes and Metallization
- High Lead Alloy Interactions – Die Attach
- Lead Free Vs. Sn/Pb Alloys – Impacts
- Over-molding Considerations

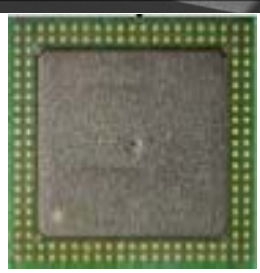
MODULE 7 – ADDRESSING PROCESS ISSUES
- Solder Balling
- Tombstoning – Math & Science
- Bridging & Opens
- Non-Wetting
- 'Black Pad' Issues
- Solder Migration
- Voids
- Fillet Lifting
- Tin Whiskers

MODULE 8 – ANALYTICAL TOOLS & TECHNIQUES
- Equipment Classification, Types & Principle Function
- Microscopy & Imaging – SEM, SAM, RI
- Surface & Metallization – Scanning Probe, AFM, MI
- Materials Behavior – TMA, MI, DSC
- Contamination Analysis – FTIR
- Analytical Equipment – SMT Application Chart

MODULE 9 – CONCLUSION
- Appendix & Glossary
- Listing of Applicable Standards
- Solder Volume Calculation Spread Sheet
- Printing Audit Guide







AUDIENCE

This workshop is suited for intermediate to high level candidates and will benefit those responsible for maintaining line yields or whose roles impact process efficiency and quality. Target industries include IC Packaging - Backend, PCB assembly, EMS/ESPs requiring skills to address their process issues and improve their end-user product user experience. This workshop will significantly benefit Engineering staff in the Manufacturing, Assembly Process and Equipment, Materials, Maintenance and Failure Analysis disciplines. Technicians or Supervisory levels with adequate grasp of SMT concepts and experience will also benefit and gain applied knowledge.

BGAs & CSPs: SOLUTION ORIENTED SMT MANUFACTURING TECHNIQUES FOR ENHANCED ASSEMBLY & YIELD

WS5 – 2 Days

COVERAGE

The objective of this program is to lay a foundation of BGAs/CSPs assembly with focus on the variables that impact their reliable attachment including an understanding of the collapse mechanism, joint formation requirements and metallurgical interactions taking place considering the vast variety of materials and metallization encountered.

The workshop will cover in-depth aspects of the BGAs, Micro-BGAs and Bumped Array CSPs, including their families, advantages, features and their assembly on the PCB and their rework processes. It will provide a detailed analysis of many process issues, steps, practical and analytical techniques that will help the participants in refining the assembly process, address specific issues and improve yields.

Key elements of the program include coverage of Non-destructive imaging techniques and their interpretation as well as metallurgical aspects relating to the solder joint and its interaction with different pad finishes. It will examine key issues such as voids, warpage, thermal stress, lead-free impacts, forward and backward compatibility and reliability of BGA assemblies. Several leading edge studies will be discussed in the class to enhance participants understanding of industry practices, approaches and outcomes.

At the end of this workshop, the participants will acquire an excellent understanding of the attachment variables, assembly requirements, assembly variants such as mirror image assembly and the process issues that may be encountered and how to trouble shoot and correct them.

OVERVIEW

Array Packaging such as Ball Grid Arrays (BGAs) and their smaller counterparts Chip Scale Packages (CSPs) and Wafer Level Packages (WLPs) are increasingly fulfilling needs that were traditionally the domain of peripheral packages. They have become defacto standards particularly in handheld and mobility products and products requiring small form factors, high-density and light weight. A variety of standard BGAs and a vast variety of array format CSPs and Wafer Scale CSPs have proliferated the market place with a multitude of form factors.

However assembling BGAs and CSPs requires specialized understanding of their unique and specific issues. Metallurgical interactions in the case of BGAs & CSPs are complex and choice of metallization plays a significant role in their reliable assembly.

An understanding of the complexities involved in their assembly is essential to meet the challenges and stay competitive in today's electronics assembly environment.

WORKSHOP AGENDA

MODULE 1 – PACKAGING DRIVERS & BGA TRENDS
- Area Array Concept Vs. Peripheral
- Technology Drivers
- Types of BGA Packages
- Types of CSPs & Structure
- Wafer Scale CSPs, Flip Chip CSPs & Variants
- BGA Families
- Foot Print Performance
- Features & Advantages

MODULE 2 – BGA & CSP ASSEMBLY CONSIDERATIONS
- Merging into Mainstream SMT Processes
- Optional Process Flows
- Key Process Control Points
- Metallurgy Interactions
- Metallization Considerations
- Gold, Silver, Tin, Nickel and Other Finishes
- Standards
- Lead Free Impacts
- Compatibility Issues – Forward & Backward
- Alloy Comparisons
- Mirror Image Assembly
- BGA Reliability Studies
- Moisture Classification & Standards

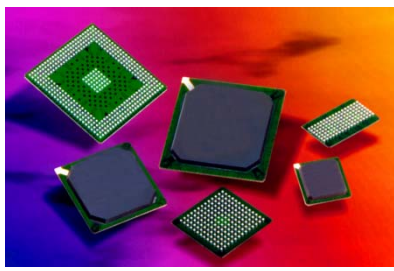
MODULE 3 – IMAGING TECHNIQUES
- 2-D Vs. 3-D X-Ray
- Tomography & Laminography
- Optical Probes & Endoscopy
- Interpreting Images & Correlation AOI

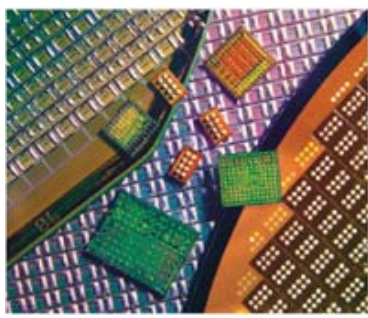
MODULE 4 – ADDRESSING PROCESS ISSUES
- Voids
- Bridging
- Warpage
- Stretching
- Opens
- Non Wetting
- 'Head-In-Pillow' Effects
- 'Black Pad' Issues
- Ball Shear
- 'Dropped' Balls
- Delamination
- Analytical Equipment for Failure Analysis & Process Development

MODULE 5 – CHIP SCALE PACKAGING
- Types of Array CSPs
- CSP Attachment
- Process Issues
- LGA & Micro Lead Frame Process Example

MODULE 6 – REWORK
- Defining Rework Strategy & Approach
- Selection of Equipment & Pre-requisites
- Developing the Rework 'Recipe'
- Developing the Profile
- Refining the Process

MODULE 7 – CONCLUSION
- Summary
- Reference Materials & Useful Websites
- Alloy Data





AUDIENCE

This Advanced Level Program requires a pre-understanding of SMT concepts. Attendees would comprise engineering level personnel from Manufacturing, Assembly, Equipment, Maintenance and Failure Analysis disciplines. However the scope of the workshop will also benefit Technicians or Supervisory levels with adequate grasp and experience of SMT concepts as well as related functions such as Vendor Quality or Incoming Quality responsible for material quality and those who have to deal with components, materials and vendor quality issues and need to have a clear understanding of how their role impacts the overall assembly process..

BRIDGING THE GAP FROM CHIP TO BOARD – LEVERAGING COB TECHNOLOGY IN SMT & PACKAGING APPLICATIONS

WS6 – 1 Day

COVERAGE

This workshop provides an in-depth coverage of Chip-On-Board in the context of SMT Assembly and Packaging. The major sections address the driving factors, COB positioning and comparisons of various approaches towards higher level of integration. The core technology of Chip-On-Board and where it is best positioned vis-à-vis other approaches is reviewed. The selection criteria and considerations for bare dies, their quality & acquisition and applicable standards are covered.

Some of the important areas included are design rules for fan out, pitches, layout, attachment considerations, process and equipment, bonding variables, bonding tools and tool variables, inspection and challenges in failure analysis and rework. Optional flows for embedding COB along with SMT Assembly on a common platform are compared in their relative merit. The vital area of metallization is emphasized with the different metallurgical systems, bonding wire and pad metallization, the resulting intermetallics and reliability impacts. Recognizing the importance of pre-bond cleanliness in many high end COB applications, especially in the field of Packaging, the section on Plasma Stripping & Etching covers the Principles, Configuration Options, Types of Equipment and Considerations for setting up a Plasma Stripping / Cleaning Process.

To help understand the concepts, the course material is rich in micro-graphs, cross sections and a discussion on closely related studies is conducted to encourage participation. An in-class microscope is used for live display of related samples. A CD ROM containing many of the pictures and references used in the program is included in the handout.

WORKSHOP AGENDA

MODULE 1 – ADVANCED PACKAGES & HIGHER INTEGRATION
- Packaging Trends & Overview
- Comparative Silicon Efficiency
- Driving factors - Products and Applications
- Die stacking , Package Stacking and TSV
- Driving Technologies - Chip-On-Board vis-à-vis Flip Chip
- SiPs and MCMs

MODULE 2 – BARE DIES
- Selection
- Quality Considerations
- Known Good Die (KGD) & Unknown Bad Die (UBD)
- Procurement Standards
- Road Map

MODULE 3 – CHIP-ON-BOARD CONSIDERATIONS
- Applications
- Positioning
- Design Rules
- Pad Design & Layout
- Design Examples

MODULE 4 – CHIP-ON-BOARD PROCESS
- Ball Bonding Vs. Wedge
- Tools & Equipment
- Bonding Variables
- Bonding Metallurgical Systems
- Intermetallics and Reliability
- Merging Chip-On-Board with SMT
- Process Flow Options - Pro's & Con's
- Reworking Chip On Board

MODULE 5 – PLASMA STRIPPING
- Principles of Plasma Stripping
- Stripping & Etching Applications
- Types of Equipment & Configuration
- Set-up Requirements
- Measuring Cleaning Efficacy
- Pull Testing
- Failure Modes and Mechanisms

MODULE 6 – CONCLUSION
- Virtual Tour of a COB Assembly Line
- Real Life Examples of COB Applications
- Summary of Key Success Factors
- References / Further Sources

OVERVIEW

Consumer, portable and mobile communication applications, the fastest growing segments of the electronics market are demanding levels of integration not supportable via mere SMT enhancements. Combining multiple dies along with surface mount components on an organic platform are amongst some of the latest approaches being used in creating multi-chip modules and other functional blocks. The approach creates complete circuit functions and all within a CSP like footprint thus eliminating or significantly reducing the burden of interconnecting separate single die packages on an SMT PCB assembly. The fact that mainstream SMT Assembly and Packaging are rapidly headed from different directions towards the common goal of greater functional integration has far reaching implications for both segments which must adapt, transform with the trends and learn from each other. There is vital need for organizations to acquire new knowledge, understand leading edge assembly processes, the issues and considerations - indeed it is a vital step ultimately determining their position in the industry.

Chip-on-Board is one of the major building blocks and core enablers (the other being Flip Chip) in the realization of higher levels of interconnection whether embedded in an SMT board or within a package. This workshop is designed to give an understanding of the approach involving COB technology whether it is over-molded into a final package or 'glob-topped' alongside SMT components.

AUDIENCE

Engineering personnel from Manufacturing, Assembly, Equipment, Materials, Maintenance and Failure Analysis disciplines. Technicians or Supervisory levels with adequate grasp of SMT concepts and experience will also benefit from the knowledge they gain. Target industries include PCB assembly, EMS/ESPs and many segments of IC packaging and Module manufacturing requiring skills to address end-user product utilization and processing issues.

IMPLEMENTING FLIP CHIP ASSEMBLY IN MAINSTREAM SMT & PACKAGING APPLICATIONS

WS7 – 1 Day

COVERAGE

This workshop provides an in-depth coverage of Flip Chip technology and its role as an enabler attaining higher levels of integration, the driving factors, pros and cons and comparisons of the many approaches and where Flip Chip is best positioned. The selection criterion and considerations for bare dies, their quality and acquisition, applicable standards and adaptability to Flip Chip specific design are reviewed in terms of impact to both manufacturers and producers.

The Flip Chip assembly process covers Design Guidelines, Options, Underfilling Considerations, Calculations & Advances and Flip Chip Reliability. Details cover a complete review of the many different types of Underbump Metallization (UBM) and Bumping processes together with Applicable design rules. Specific applications such as Flip Chip on Glass (FCOG), its various attachment modes and Flip Chip on Flex (FCOF) are given full coverage. Important failure modes such as Electromigration, Current Crowding and Diffusion Failures are explained as are the techniques for Failure Analysis.

To help participants understand the concepts the content is rich in micro-graphs, cross sections, videos and engineering studies. An in-class microscope is used for live display of related samples. A CD ROM containing many of the pictures and references used in the program is included.

WORKSHOP AGENDA

MODULE 1 – ADVANCED PACKAGES & 3D STACKING

- Packaging Trends & Overview
- Comparative Silicon Efficiency
- Driving factors - Products and Applications
- Die stacking and Package Stacking
- Driving Technologies - Flip Chip vis-à-vis Chip-On-Board
- SiPs and MCMs

MODULE 2 – BARE DIES

- Selection
- Quality Considerations
- Known Good Die (KGD) & Unknown Bad Die (UBD)
- Procurement Standards
- Road Map

MODULE 3 – FLIP CHIP DESIGN GUIDELINES

- Bump Pitches
- Bump Heights
- Array Vs. Peripherals
- Under Bump Metallization (UBMs) and Design Rules
- UBM Parameters
- Bumping Processes
- Bump Shear Strengths

MODULE 4 – FLIP CHIP ATTACHMENT

- Merging with SMT Process
- Process Flow Options
- Understanding Underfills
- Underfilling Trends
- Developing & Qualifying The Process

MODULE 5 – FLIP CHIP RELIABILITY & ANALYSIS

- Reliability Factors
- Failure Mechanisms & Modes
- Electro-migration & Current Crowding
- Shear vs. Ball Pluck Testing
- Micro-sectioning – How To's

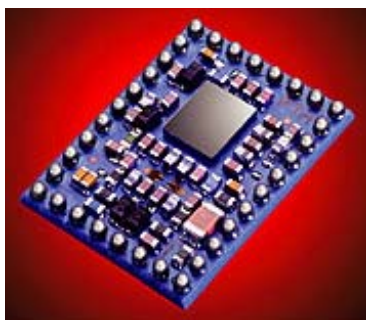
MODULE 6 – CONCLUSION

- Summary of Key Success Factors
- Further Sources of Information & References

OVERVIEW

Traditional SMT assembly is being permanently transformed with the move towards 3D applications, Package-on-Package (PoP) and other forms of stacked interconnection. Consumer, portable and mobile communication applications are amongst the main driving engines behind this move demanding constantly higher levels of integration. Die and package stacking approaches combine multiple dies with capability of creating complete circuit functions within a CSP footprint thus eliminating or significantly reducing the burden of interconnecting separate single die packages on an SMT PCB assembly. Flip Chip is one of the principle enablers in this goal whether embedded in an SMT board or within a package.

Application specific variations such as Flip Chip On Glass (FCOG) have enormous potential given the explosive growth of LCD panels and other display applications and need to be understood. This workshop is designed to give an understanding of the core technologies of Flip Chip, Flip Chip on Glass (FCOG) or Flex. Mainstream SMT Assembly and Packaging segments both deploy the Flip Chip approach in high performance, high speed and high density applications. There is vital need for organizations to acquire and understand the Flip Chip assembly process, the issues and considerations - indeed it is an important step towards sustaining growth in a rapidly transforming environment.



AUDIENCE

This is a high level program to address the needs of a range of industries that are either involved with or getting prepared for advanced packages and interconnection techniques in SMT assembly. It will also greatly benefit many back-end and packaging areas that deploy Flip Chip technology in the manufacturing of advanced packages.

The target audience would comprise experienced personnel from Engineering, Process, Manufacturing, Assembly, Failure Analysis and Quality disciplines.

SOLDERING METALLURGY – SCIENCE & PRACTICE IN SMT PROCESSES

WS8 – 1 Day

COVERAGE

The objective of this session is firstly to lay down the foundations and fundamentals of metallic alloy systems, metallurgy and alloy properties and how they impact the solder joint. With this foundation, the soldering process can then be better understood in an objective and analytical manner. The workshop will cover the requirements for the formation of the solder joint with different plating technologies and soldering materials with emphasis on Lead Free materials and the impact of cooling rate on crystallization and nucleation ability on the final joint appearance. Modern plating finishes and their interactions with solder, the resulting intermetallic phases and their physical and mechanical properties and the impact on joint reliability will be covered. High Lead solders metallurgical interactions will also be reviewed for the benefit of the packaging professionals.

The workshop will also cover the assessment of solderability, the different types of fluxes as well as issues such as 'Black Pad' defects. Participants will learn how to resolve soldering issues encountered in Reflow and Wave processes. Real life examples of soldering issues under different scenarios will be presented. The workshop will also touch upon Tin Whiskers and some of mitigation practices being used in the industry.

The participant can expect to emerge from this workshop perceiving the soldering process at a much higher plane, to grasp and to open their mind to the vast range of interactive variables, able to address soldering issues as well as apply the know-how learned in dealing with the wide range of metallization applications and interactions

OVERVIEW

One of the most challenging areas faced by the SMT engineer relates to the metallurgy of soldering and understanding the behavior and interactions of different metallization encountered in the SMT process. Invariably the SMT professional is not a metallurgist by background and therefore an understanding of applied metallurgy becomes vital since metallic interactions are very specific in the case of SMT processes. The situation is made complex by the multiple alloy systems in any soldering process. With the advent of Lead Free soldering and multiple alloy choices the variables have become even more complex. Other areas such as packaging continue to use high lead solders as die attach or solder bump interconnect materials for Flip Chip in package applications with their own set of interactions. In this workshop Metallurgical interactions are dealt with in the light of current and emerging trends, solders, plating and materials with emphasis on their relationship to soldering issues, their objective assessment and resolution.

WORKSHOP AGENDA

MODULE 1 – ALLOYS & SOLDERING
- Primary Materials
- Alloy Definition
- Soldering Definition
- Alloy Systems Involved In Soldering

MODULE 2 – CRYSTALLIZATION & NUCLEATION
- Microstructures
- Microstructure Transformations
- Equilibrium Phase Diagrams
- Nucleation and Grain Size
- Impact of Cooling Rates on Grain Size

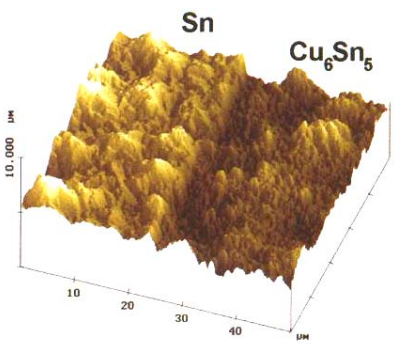
MODULE 3 – COMPONENT RELATIONSHIPS
- Solid Solutions
- Eutectics and Eutectoids
- Electron Compounds
- Intermetallics Morphology and Properties
  - Tin Cu
  - Tin Gold
  - Tin Silver
  - Tin Nickel
- Ternary Intermetallics
- Intermetallic Growth Rates Comparison
- Diffusion Rates of Common Soldering Metals

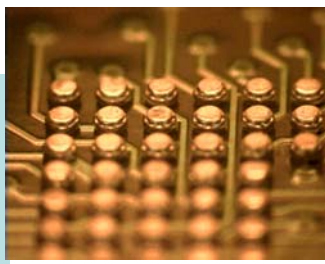
MODULE 4 – METALLIZATION FINISHES & PROPERTIES
- Metallization Options – Comparisons, Pros/Cons
  - Gold Plating
  - Tin Finishes
  - OSP
  - HASL
  - Electroplated Nickel
  - ENP
  - ENIG & SENIG
  - Immersion Silver
  - ENEPIG
  - DIG
- Solderability Testing and Standards
- 'Black Pad' Defects Understanding
- Tin Whiskers

MODULE 5 – SOLDERING ALLOY PROPERTIES
- Mechanical Properties of Alloys
- Strength Testing
- Sn Pb Vs. Pb Free Alloys
- Physical and Mechanical Comparisons of SnPb Vs. Pb Free Alloys
- Wetting Properties of Different Alloys
- Alloy Options & Impact On Joint Reliability

MODULE 6 – ADDRESSING SOLDERING ISSUES
- Solder Balling
- Bridging & Opens
- Non-Wetting
- Solder Migration
- Voids
- Fillet Lifting
- Wave Soldering Issues
  - Dewetting
  - Skips
  - Hole Fill

MODULE 7 – CONCLUSION
- Summary
- References
- Useful Websites





AUDIENCE

This workshop is suited for intermediate to high level candidates and will benefit those responsible for maintaining line yields or whose roles directly impact such yields and requires an in-depth understanding of solderability and the resolution of solderability related issues, specifying materials, and defining processes. It is recommended that the participants have at least a year or more of line experience and have an understanding of all of the various assembly processes. The target audience would comprise Manufacturing and Assembly line functions, Failure Analysis Engineers and related functions such Vendor Quality or Incoming quality responsible for material quality and those who have to deal with components, materials and vendor quality issues.

TIN WHISKERS –
RISK ASSESSMENT & MITIGATION STRATEGIES

WS9 – 1 Day

COVERAGE

The objective of this workshop is two fold. Firstly the workshop will lay a foundation and understanding of the Tin Whiskers, their morphology, microstructure and review the risks and extent of impact on the end product. The course will review the historically studied growth mechanisms and conditions including the impact of the environment and compare the various investigations and growth propositions. The second part of the workshop will deal with the mitigation aspects and strategies for whisker management including, for example, the extent and useful of conformal coatings to mitigate whisker impacts.

Apart from the various proposed growth mechanisms for Tin Whiskers this workshop will examine various measures being used by the industry and their usefulness, such as the interactive effect of stress factors, effects of plating parameters, substrate preparation, substrate materials and environmental influences. In addition, the effects of plating thickness, under layers, post-plating annealing, plating structure and alloying agents on Whisker growth will also be presented and explored. A large number of micrographs depicting the structure of Tin Whiskers and also of Real Life failure modes will provide further insight and knowledge.

It is important that effective and low cost strategies for controlling Tin Whisker risks being adopted be assessed and ranked for reliability. As of date Pure Tin is NOT a recommended finish by key Industry Standards for High reliability electronics. Many of the pitfalls, myths and realities involved, do's and don'ts and process control recommendations including for instance design aspects, packaging, storage and handling and their impacts will be presented. Mitigation strategies will be discussed as well as a coverage of conformal coatings. Many micrographs will be used throughout to enhance the understanding and a wide variety of studies from key segments of the industry will be reviewed both from an information and findings standpoint as well as for the participants to use as reference materials.

WORKSHOP AGENDA

MODULE 1 – OVERVIEW OF TIN WHISKERS
- Historical Perspective
- What Are Tin Whiskers
- Nature of Tin Whiskers
- Problems Associated With Tin Whiskers
- Impacts on Products & Micro-Circuits
- Reliability Risks
- Failures - Real Life Examples & Experiences

MODULE 2 – WHISKER GROWTH MODELS
- Observed Structures & Morphology
- Review of Various Lab Studies
- Proposed Models of Growth – Current state of knowledge
- Macro Stress – Evaluations
- Micro-stress
  - Intermetallic Growth
  - Solid State Diffusion
  - Low Micro-stresses
  - Dislocation Mechanisms
  - Secondary Whiskers
  - Grain Boundaries Impact
  - Voiding

MODULE 3 – STRATEGIES
- Metallization Impacts
- Stress Alleviation
  - Plating Thickness Considerations
  - Plating Under Layers
  - Annealing
  - Design Factors
- Storage & Environmental Factors
- Progressive Impacts of Growth Factors
- Thermal Cycling Impacts
- Conformal Coatings – Studies & Recommendations
- Lead Spacing Vs. Risk
- Control Approaches By Applications

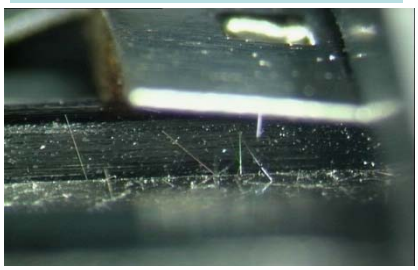
MODULE 4 – CHALLENGES IN TIN WHISKERS
- Open Issues Facing The Industry
- Consistencies & Contradictions
- Industry Initiatives – The Road Ahead
- Whisker Evaluation – Review of Standard JESD 221

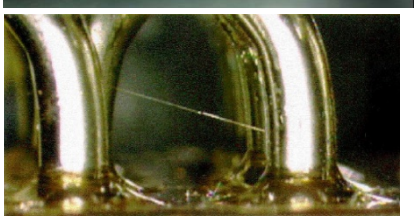
MODULE 5 – CONCLUSION
- Summary of Growth & Mitigation
- Future Reading
- References

OVERVIEW

With the world-wide transition to RoHS compliant electronics, the industry has for the vast part converted their metallization to Lead-Free finishes. Although pure tin is a predominant choice for a lead-free metallization, it poses the challenging issues of Tin Whiskers. As of date Pure tin is NOT a recommended finish for High reliability electronics. Tin Whiskers have been found to form on a wide variety of tin-plated component types and PCB pads under a range of environmental conditions. Tin Whiskers comprise nearly pure tin, are electrically conductive and can cause shorting of electronics and other issues in the finished product as well as in micromechanical systems.

The growth of whiskers has been attributed as a cause of reliability problems for electronic systems that employ metallization plated with tin. Manufacturers of high-reliability systems and other high-end users have not been immune to these issues. Field failures attributable to Tin Whiskers have cost many millions of dollars and become a leading cause of customer dissatisfaction. The industry has been grappling this known problem for many years and even today the complexity of the mechanisms are still being uncovered. Over the last few years, much energy and renewed effort has been put into this subject and the latest findings and strategies for control are now becoming available. Even as further work continues, it is vital for manufacturers to remain abreast of emerging developments and deploy the latest technology in their field.





AUDIENCE

This is a high level program and requires a pre-understanding of SMT concepts. An understanding of applied soldering metallurgy will be helpful. The target audience will comprise personnel from Engineering, Process, Manufacturing, Assembly and Failure Analysis disciplines. It is a vital and highly beneficial course for those involved in the conversion to lead free processes. The audience scope can be extended to include experienced Technicians or Supervisory Level staff with adequate knowledge of SMT concepts. Vendor Quality and/or Incoming Quality personnel responsible for quality management of components, materials and vendors may also gain vital information needed for vendor quality programs and strengthen their respective function.

ABOUT THE INSTRUCTOR

MUKUL LUTHRA

BUSINESS DIRECTOR & FOUNDER – WATERFALL TECHNOLOGIES

Mukul Luthra graduated with a Degree in Electrical Engineering in 1974 and has extensive experience in the electronics industry. With over 35 years of High Tech experience, in Singapore, the US and Canada, he is a leading Professional Trainer and Consultant known for his process expertise – high volume manufacturing, quality & process engineering in the PCBA, Disk Drive and Semiconductor industries. He wrote the *Rim Watch* column on *SMT* issues for several years in *Circuits Assembly* Magazine and continues as a technical writer. To-date, Mukul has consulted 40% of the world's leading electronics manufacturers.

He has over 40 papers, articles and features published, has chaired and presented at numerous international conferences and conducted workshops at the IPC/APEX, SMTA International, Nepcon and GlobalTronics events.

Mukul is CEO of Waterfall Technologies. Amongst the previous positions he has held include Marketing Director, ST Microelectronics and Director, Seagate Technology. Waterfall Technologies has trained hundreds of professionals over the years in almost every major Multinational and Small and Medium Enterprises involved with PCB Assembly. Developing SMT professionals through training, hands-on problem solving and process involvement is their core competence and primary mission. The training program and services offered are world class and on the leading edge of technology.

CERTIFICATES

Each participant will receive a Course Completion Certificate at the end of the workshop to demonstrate their professional dedication and commitment to their field.

WORKSHOP FEE

All our On-site workshops are affordably priced. There is a fixed fee for up to the 1st 15 participants and a nominal add-on fee for additional participants. Maximum recommended class size is around 35. Waterfall Technologies can also organize the entire training program as a package at a venue of your choice.

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What our Clients say about our programs ....

"Excellent Trainer Knowledge and Delivery; very in depth subject" *"Good information provided to allow use of key factors in possible problem solving.."*	**BENTLEY MOTORS, UK**
"Very detail information, filled with sheer knowledge. Brilliant detailed presentation"	**Fairchild Semiconductor**
"Very informative on latest semiconductor technology roadmap"	**ASE Electronics**
"It was a great workshop and a very good presenter, a well experienced"	**Agilent Technologies**
"Good – I learned a lot from this workshop & exposed to new things" *"Interesting & attractive course with a lot of case studies and pictures to share with participants"*	**National Semiconductor**
"Up to date and very informative"	**Sony EMCS**
Wide information on BGA characteristics"	**Lemtronics**
"Good knowledge and lots of idea on how to enhance SMT processes"	**Flextronics**
"Fantastic presentation and I gained vast knowledge in this training"	**Solectron**
"Instructor demonstrates deep technical knowledge and excellent technical capability" *"One of the most convincing technical training I have attended"*	**International Rectifier**
"Mukul is very knowledgeable in a large range of topics and he has a very good presentation skills"	**Unaxis Singapore**
"Solid presentation and excellent technical know-how"	**Dominant Semiconductor**
"Instructor is very well prepared"	**Micron Semiconductor**
"Very informative, very detailed explanation and practical to apply what has been taught at work"	**Pepperl + Fuchs**
"Very well prepared, capable and experienced facilitator"	**Nationgate Technology**
"Well organized and highly informative. Excellent speaker"	**Mitsubishi Electric**
"Overall is beyond my expectation. A really good workshop"	**KESM Industries**
"Interactive presentation with good sample of packages to share with the class"	**Speedy-Tech Electronics**
"I thoroughly enjoyed the workshop, very interesting and fruitful information"	**DEK Asia-Pacific**
"Perfect, very interesting and useful course. Well done"	**Ibiden Singapore**
"Mukul displayed expertise and passion during the presentation, a job well done!" *"Presentation was well organized and informative. Made it easy for us to understand."*	**Pacific Insight Electronics Nelson, BC, Canada**
"Very informative, well-planned and presented! Any eye-opener for me" *"Very good presentation material, moving forward …"*	**VistaPoint Technologies**