

# Process challenges and solutions for embedding chip-on-board into mainstream SMT assembly

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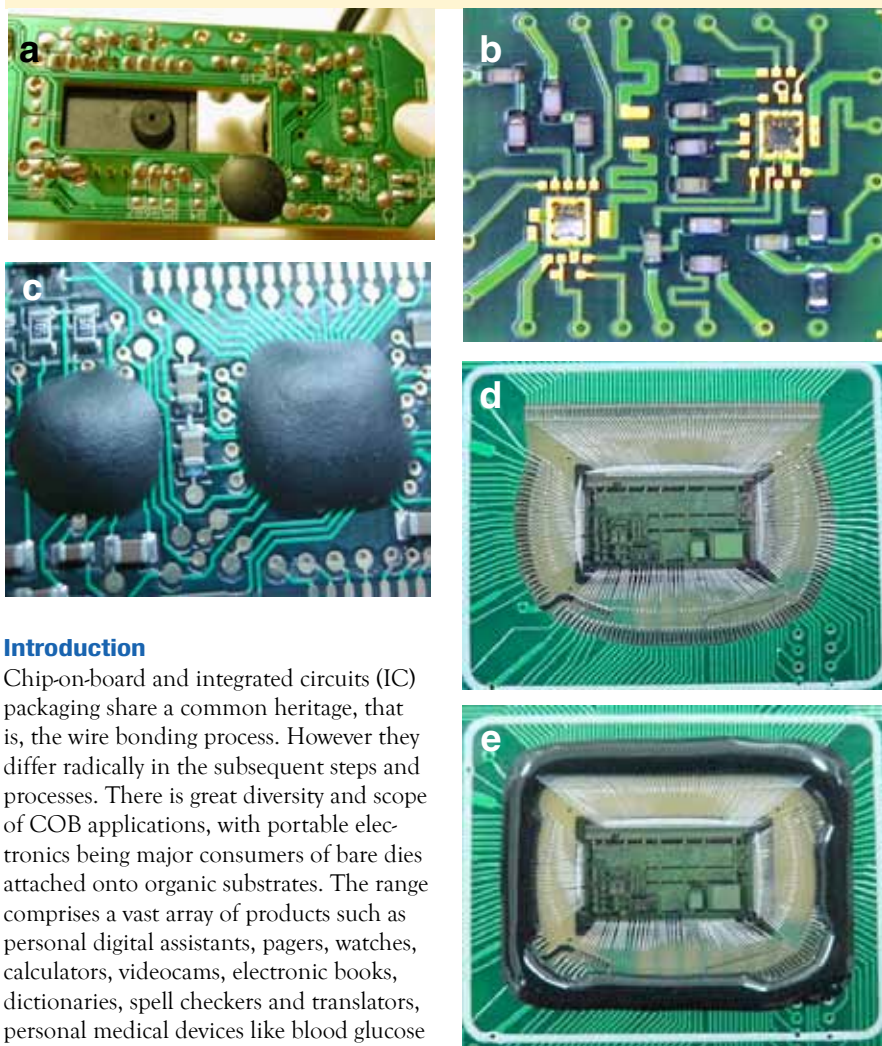
Merging COB into mainstream surface mount processes significantly improves footprint efficiency and cuts cost and lead-time, but it has also usually entailed acquiring specialized know-how through considerable 'hands-on' experimentation.

This paper provides the required information on all aspects of the COB process from applications, positioning, costs, die selection, layout, process options, equipment and rework for implementing COB processes into existing SMT lines and manage COB yields. Based on real life examples, the paper covers the key considerations, major critical factors and the challenges for a successful COB-SMT merge

**Keywords:** Chip On Board, COB, Surface Mount, SMT

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Figure 1. a) COB in a PC mouse application. b) High I/O COB die in a portable application. c) COB devices in a heart rate monitor. d) COB in a SiP (RF) application. e) Same die as in d, shown with dam.



## Introduction

Chip-on-board and integrated circuits (IC) packaging share a common heritage, that is, the wire bonding process. However they differ radically in the subsequent steps and processes. There is great diversity and scope of COB applications, with portable electronics being major consumers of bare dies attached onto organic substrates. The range comprises a vast array of products such as personal digital assistants, pagers, watches, calculators, videocams, electronic books, dictionaries, spell checkers and translators, personal medical devices like blood glucose testers, hearing aids and other monitoring devices apart from a wide range of toys and handheld games. Other applications include caller identifier devices (ID Chip sets) & cordless phones. Radio frequency

(RF) modules use gold wire or ribbon bonding of gallium-arsenide (GaAs) devices without encapsulation on ceramic or Teflon substrates. Chip on board can be

found in common every day products such as a computer mouse (Figure 1a) or in many home appliance display panels. Other applications include chip on flex which enables folded assemblies adaptable to a complex end product form factor.

One or two COB devices per assembly are routine, but products may use as many as six COB devices on one board. COB is essentially the grass-root technology behind many plastic ball grid arrays (PBGA), array chip-scale packages (CSP), systems in package (SIP) and many package-on-package (PoP) and package-in-package (PiP) approaches. Multiple stacked dies wire bonded on organic substrates alongside other surface mount devices are now common place. Figures 1b to 1d exemplify the scope and range of COB.

### COB positioning

The cost per pin for the more traditional packages like quad flat packs (QFP) and small outline (SO) ICs has flattened out at around the 0.25-0.5 cents mark, depending on size and volume. One reason is that traditional IC packaging and test equipment has already been amortized over the years. The other is the astronomical volume. By comparison, prices for some of the newer packages, like lead-frame CSPs, may range between 0.4 to 1 cent per lead and 0.5 to 1 cent per sphere for a laminate version CSP (all excluding die costs). For COB, the cost per I/O charged by a board assembler comes in equal or marginally higher than the equivalent cost of packaging and testing the same die in a traditional package. This, however, hides the real savings. The large die in Figure 1b, has around 184 bonds and would have likely fitted in a 28 mm x 28 mm QFP. Bypassing the IC package saves nearly two-thirds of related PCB real estate.

COB is also well positioned to serve in applications where packaged devices are simply too large to fit, and that require the space saving and low profile feature but not necessarily the footprint efficiency or speed performance of a flip chip.

As example, Figure 1c shows two COB devices on a board of around 25mm diameter in a wrist-worn, heart rate monitor application.

A major intangible factor in favor of COB is the reduction in lead-time. With COB the board assembler procures dies straight from the fab house, cutting out packaging and testing, saving weeks on IC lead-time. Time to market can be a major success factor and, combined with real estate savings, easily offsets the modest delta cost of the COB process.

This is particularly true of products in a fast moving market segment where cost effectiveness and being ahead are key to their marketability.

### Die quality & cost perspective

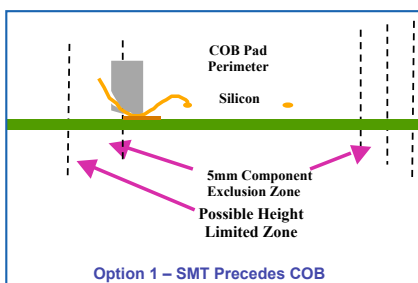
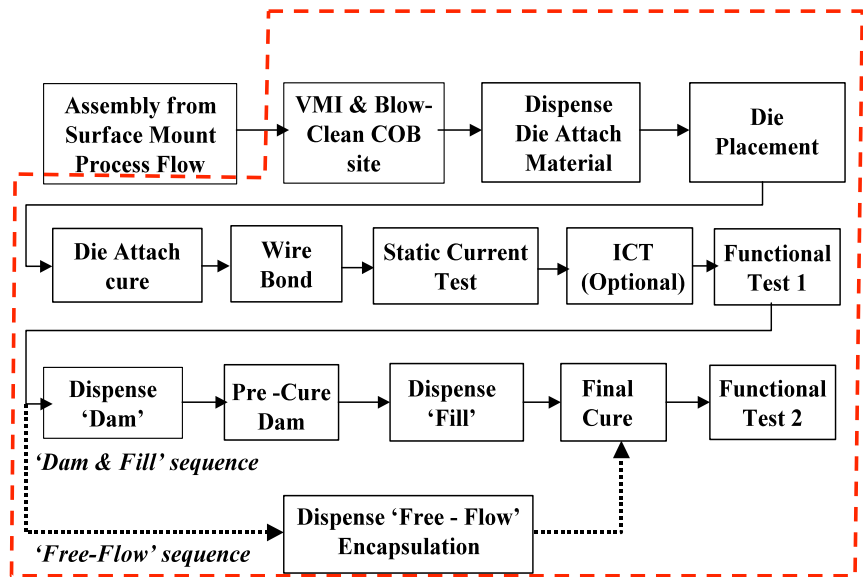
Die quality impacts on final assembly are an important consideration for an assembler. Electrical Probing at wafer level (EWS) has limitations that seldom yield confidence levels at par with exhaustively tested and burned-in ICs<sup>1</sup>. IC-level quality and reliability assurance poses challenges to implement at die level and certainly so at the consumer's price expectations. The true intent of the known good die (KGD) standard, that bare dies equal packaged IC quality and reliability, falls short of reality.

Escalating demand for bare dies, however, continues to be a driving force, leveraging pressure towards reduction in UBD within a KGD population. Measures such as temporary die test carriers can and are being used but such measures must be deployed selectively as they are costly and also not completely free from the risk of die damage. Wafer level burn-in to detect die infant mortality and improve reliability has come a long way

but proves too costly for low to mid cost COB usage. In a nutshell, major hurdles center on maintaining die integrity at a price point commensurate with the end target application. Although UBD defect levels have reduced over time, there's still a march ahead.

Die selection for COB requires accepting and dealing with the reality of unknown bad dies (UBD) within the so-called KGD population. UBD are defective, congenitally weak or marginal and may fail during subsequent COB processes. Despite the decade old SIA envisaged milestone at or below 100 parts per million (PPM) UBD defectives the industry average is not quite there. If the KGD program compliance relies purely on die yields, the dependency variables—process technology, die size and complexity, wafer diameter and foundry maturity must all be considered.

The EIA/JEDEC standard JESD49<sup>2</sup> covers requirements for information on die procurement but leaves considerable leeway for supplier discretion on data. Die yield data is usually kept proprietary and it's the very data the assembler needs! Even as progress is being made, the board



assembler must be prepared for defective dies and process yield loss.

In the denouement, COB is well suited to the low end short life cycle products targeting consumer or commercial grade applications using sub dollar or at most \$2 per die. The COB approach is too risky and not robust enough for industrial or high reliability applications involving high \$ value ASICs or complex VLSIs which are hard to test or assure even as packaged ICs.

### Die sizing and I/O considerations

Dies used for COB on surface mount assemblies should typically target under 200 wire bonds/die. Smaller dies form more reliable candidates for COB due to the inherent Cte mismatch between the die (Si: 2.3 PPM/°C) and the substrate (Fr4: 18-25 PPM/°C). Similarly, small signal devices fare better than do those dissipating heat as in power applications. Large sizes increase probability of ‘popcorn’ effects if the COB is subjected to reflow thermals; the assembly behaves quite like packaged ICs. Die sizes are application dependent. Some of the larger dies encountered by the author, for instance, are 270 mils by 300 mils (81 kmils sq.) and 350 mils by 350 mils (123 kmils sq.). These dies have Pad sizes of 3 mils by 3 mils (75 by 75 microns) and interpad pitch of 4 mils (100 microns). Liquid crystal display (LCD) drivers, some application specific ICs (ASICs), microprocessor units (MPUs) and microcontroller units (MCUs) lend themselves as good candidates and are routinely encountered in COB applications.

### Process considerations

Figure 2 illustrates the process flow where

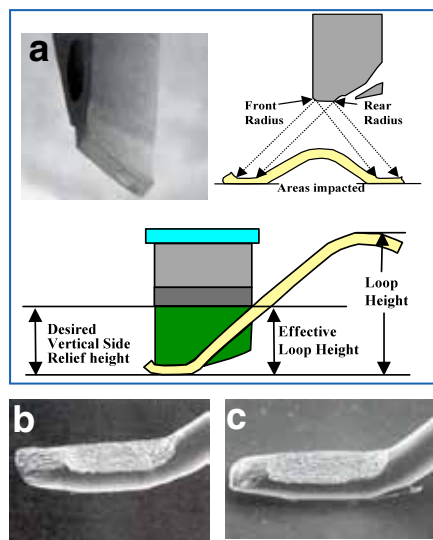


Figure 3. a) Wedge tool profile parameters. b) Flat footprint. c) Concave footprint.

SMT precedes the COB. The dotted red line shown encases the clean room assembly portion. Discussed below are some of the salient considerations and key factors for a successful SMT-COB merge comparing 2 different options—SMT before or after COB.

#### Option 1:

In this option the surface mount assembly precedes the COB process and it is considered by default as the preferred option. Although not shown in its entirety in Figure 2 the surface mount process follows traditional assembly steps and may be full DS surface mount or mixed followed by the COB process. The advantages with Option 1 are that it protects the COB from reflow soldering thermal excursions (and stress) and is friendly for Paste printing. The downside is the increased board contamination potential, which could lead to bonding issues namely lower intermetallic percentage (IP) coverage and marginalized bond strength. With maturity, contamination can be managed. However Option 1 requirements of a component exclusion zone and a height restriction zone around the COB site are tradeoffs which must be accepted.

#### Option 2:

In exceptions when the design or layout of the board is not ideal, and the COB process must precede the surface mount. The major issue is when the bonding tool interferes with other surface mount components around the COB site due to tight spacing and insufficient clearance. One alternative is to use deep access bonding (expensive); the other, do COB first.

Option 2 complicates paste printing. As shown in the diagram, the printing stencil needs a large opening in the COB encapsulated area. This opening must be sealed with a film like membrane, thin enough to adapt to the COB form and yet durable to the rigors of thousands of print cycles. Polyamides films have been used as one option and dimpling of the stencil is another but both methods have severe limitations. Furthermore the squeegee design must deal with conflicting requirements of adapting over the protrusion yet printing uniformly everywhere else. Overall, the printing is marginalized with poor gasketing, excessive paste bleed-through and deposit inconsistency around the COB area. Selective printing is possible only if layout permits but it does rob process efficiency. Alternatively, paste may be dispensed at effected sites but is inefficient and

precision dispensers are costly. Option 1 remains the preferred sequence giving easier to manage tradeoffs.

### Wire bonding and equipment

Of the principle types of bonding, two-gold ball bonding and gold wedge bonding find applications at the higher end, in industrial, RF modules and in component manufacturing such as lead frame ICs, BGAs and many CSPs. Both require substrate heating to 200°C or higher, depending upon type. The third—aluminum silicon (AlSi) wedge bonding—is well suited and prevalent in COB applications. Al wire is cheaper and bonding accomplished at room temperature, making it ideal for organic substrates while minimizing die stress. Wedge bonding tools need to be ground very narrow for fine pitch capability but their form can lower loop height, an important consideration for low profile applications. Wedge bonding tools for Al wire are cheaper than those for gold wire (tungsten carbide versus titanium carbide respectively). However, wedge bonding tools must maintain bond-to-wire orientation so the job or tool must rotate, making it slower.

Critical factors are controlling heel cracks and footprint shape, both relating to tool shape and maintenance. Figure 3a shows a typical wedge tool with some of the significant profile considerations such as the desired vertical relief height, wire loop height, effective loop height and hole shape (round or oval). Other significant tool considerations are the footprint—flat or concave (Figures 3b and 3c)—the effect of back radius (BR) and front radius (FR) and the wire angle. These interactive variables must be optimized to obtain the desired bond characteristics, bond strength and in controlling heel cracks which occur due to crystallization and hardening at the wire-footprint junction. A sharp wire transition angle, for example, can lead to fractures. The obvious cracks can be detected—it’s the latent ones that cause grief, giving test intermittence and reduced thermal cycle life. Bonding tools require effective cleaning and maintenance programs and tool life runs typically around 400 K to 700 K bonds.

Bonders are judged on bond quality, key selection considerations being bond time; force and power range programmability, type of bonding, vision system & pitch capability, speed and cost-performance. Prices run from around \$65 to \$200k depending on bond type, pitch and thruput capability. Table 1 documents some typical equipment specifications and

capability.

### Die placement and attachment

Dies are supplied either in wafer form requiring mounting and dicing or as pre-diced wafers on tape for auto die-attach machines or for pick-&-place onto die carriers. A common mode, pre cut dies in 'waffle trays' as in *Figure 4*, are well suited for semi-auto or manual assembly.

Moisture sensitivity mandates the storage of raw dies/ wafers in temperature- and humidity-controlled dry cabinets with nitrogen purge. The process environment too must be well controlled since Epoxy coated die will absorb moisture once removed and must be encapsulated within 24 hours.

Die attach materials are typically silver filled single part epoxies. Important material selection criterion include excellent thermal and electrical conductivity, viscosity and rheology to minimize tailing and stringing during dispense. Automated dispensers may be justifiable if dictated by end product precision and thruput requirements. Manual assembly relies mostly on skilled operators using time and pressure method dispensing, the dispense pattern being a diagonal cross.

Die placement can be automated if justified. A typical wafer-form die pickup & attach machine averages around \$120K. In manual applications, dies are typically picked from 'waffle trays' by a rubber tipped vacuum pen. A skilled operator assisted by 3-diopter magnification can achieve the placement accuracy needed in about 30 seconds/die. Any XY and  $\theta$  shifts are adjusted out by the bonder's vision system, referencing off alignment marks and die outline. Dispensing and die placement needs visual inspection both pre and post die attach cure. Most critical at this stage is pick-up tool tip maintenance and control of die tilt. Damaged and contaminated pick-up tips can trash a lot of dies quickly. Post-cured die tilt of even a few mils may create pattern recognition problems leading to misbonding.

### Metalization, layout and clearances

A comprehensive coverage of metallization options for Optimum COB is quite beyond the scope of this write-up and is covered in a separate sister paper<sup>3</sup>. For AlSi Wire bonding the copper is plated over with 75-100 micro inches of nickel followed by with 3-4 micro inches gold flash. Nickel (Ni) alone is also used in many low end applications. For gold wire bonding 10-20 micro inches gold plating

is preferred which favors wire bonding but is not suited for soldering due to excessive tin-gold intermetallic precipitation at the solder to metallization interface. This imparts brittleness making solder joints prone to fracture failures. End product cost is important deciding factor. The generally accepted trade off at the low end is thin gold. An expensive option for higher end applications is selective plating which provides a gold thickness optimum for both soldering and bonding.

Following real life parameters from the die in *Figure 1b* demonstrate layout considerations:

Min Die Pad Pitch = 4 mils (100  $\mu$ )  
 Pad Die size = 3mils by 3 mils (75  $\mu$  by 75  $\mu$ )  
 Min PCB Pad size = 5 mils by 20 mils.  
 (This Pad length allows re-bonding room in case of rework)  
 Min PCB Pad Pitch = 10 mils  
 Max Wire Length = 200mils  
 Wire Diameter = 1mil  
 Wire Loop Height = 5-15 mils  
 Max. Die to PCB Pad Wire Angle = 45 Degrees (to prevent wires crossing adjacent die pad)

**Clearances: Option 1** flow needs both a no-component zone and a height limitation zone around the COB site to allow the bonding tool to operate safely. Clearance requirements are machine and tool specific and determined from machine specs. **Option 2** flow needs a minimum 5 mm no component zone around the COB post-encapsulated site.

### Contamination control

The COB assembly requires a class 10k or better clean room, bunny suits, facemasks and clean room handling discipline and control. However all processes must be examined for contamination potential. Reflow ovens should be meticulously clean of micro solder balls and flux residues. Any offline operations, involving human contact are suspect sources of organic contaminants. Ultrasonic bonding energy is sufficient for normal oxide films and tarnish but not for excessive amounts of contamination. Plasma etching is needed to obtain the requisite bond strength and reliability for high-end applications, Disk drive COF and in BGA assembly. Plasma stripping is a more aggressive option being used currently in many IC assembly operations deploying the COB process.

Frayed edges of punched PCBs can shed fibers on the board surface leading to misbonds, so an effective tool sharpening

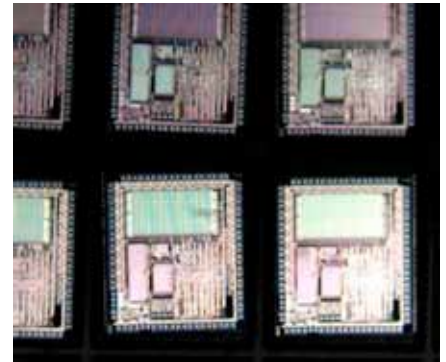


Figure 4. Waffle tray.

and control program must be in effect at the raw fab house. Pre bond blowing with dry air or nitrogen (N<sub>2</sub>) assists in micro debris and particulate removal. The discerning COB assembler opts for routed PCBs over punched.

### Bonding parameter control

Bond power, time and force settings are bond type and application dependent and critical during machine set up. The Ultrasonic energy must be enough to bare the active metals for intermetallic bonding and yet maintain die integrity. Excessive bonding energy can lead to die stressing, cracking and cratering issues, some of which may surface during reliability testing.

*Figure 5* shows the interactive wire bonding variables. One can readily appreciate the complexity of the process and the need for continued education! A complete treatise on all the interactions is beyond the scope of this write-up. Optimization of the variables is best done through design of experiments (DOE). The final measure of bond quality and reliability is bond strength. Aspects relating to bond strength and its measurement are defined under the Mil. Std. 883 D method 2011.7, which is useful for initial qualification and for ongoing statistical process control.

### Testing

The Process flow (*Figure 2*) shows the need for pre-encapsulation tests, which comprise a total static current test validating basic connection and die integrity followed by a functional test (FT1). Following FT1, protective encapsulation is applied over the COB and cured. A critical factor is allowing the post-encapsulated assembly to cool and stabilize prior to the 2nd functional test (FT2), essentially a repeat of FT1, to ensure post encapsulation bond integrity. Careless or excessive handling of the hot assemblies immediately following cure may cause bond failures. This three-step

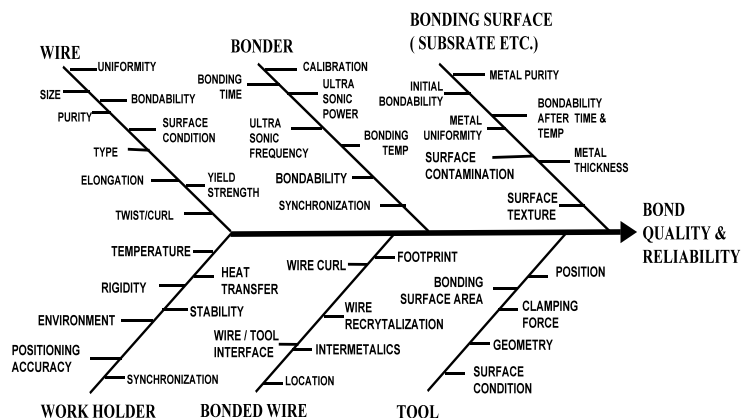


Figure 5. Wire bonding fishbone diagram.

test regimen improves finished assembly test yields and moves fault detection to the pre-encapsulation stage where COB rework is easier. Upon process maturity, FT 2 may yield levels high enough to skip it altogether. The test regimen works for either flow—SMT before or after COB. With SMT before COB the test fixtures are simplified since the assembly is essentially complete. In case of SMT after COB (Option 2 flow) test fixtures need an auxiliary board with just the SMT components (minus the COB devices) connecting to the COB assembly under test via test pins. FT can be made simple or as thorough as needed depending upon the completion level of the assembly. ICT of the assembly is a nice option, and preferred, but feasible only if the assembly is designed for it and provided the value-add justifies ICT equipment cost.

**Encapsulation options**

Many COB encapsulation materials are single part epoxies similar to those used in the semiconductor packaging industry. The critical selection criterions are Rheology, Glass temp T<sub>g</sub>, Coefficient of thermal expansion (Cte), low ionic contribution, easy cure and post cure protection properties. Thermoset coatings require typically 3-6 hrs at 140-120° C curing. Ultra Violet (UV) curable rivals are coming along, claiming improved protection.

A 'glob top' (GT), as the name applies, is obtained by a free flow of high viscosity coating. GT is easier but suffers from footprint and consequential height variability and suited for less critical applications. Control of encapsulation height is crucial for reliability. Too close to the bond wire loop or wire exposed causes failures. Precise height and footprint require an auto dispenser using Archimedes valve or positive displacement

methods and can cost up to \$300K. Dam and fill (D&F), seen in Figure 1e, lays down a contiguous high viscosity bead, creating a well-defined containment. This 'dam' is pre-cured typically for 2-5mins. The 'fill' is low viscosity spiral pattern using precise dispensing guidelines. Encapsulant materials must be preconditioned and the board temperature elevated to around 80° C to minimize air bubbles and moisture entrapment to prevent 'popcorn' effects.

**Failure analysis and improving yield**

Failure analysis poses the most challenges amongst all the steps in COB assembly. Die level visual inspection can, however, be learned and is accomplished at 50-500 X to detect fab defects and surface damage. Mil. Std. 883 E, method 2010.10<sup>3</sup> defines the visual criterion governing bare die acceptance.

Mounted and bonded dies can be removed; the Al wires and pads chemically etched to expose the underlying Silicon and visualized for cracks and damage causing leakage currents. Once encapsulated, analysis becomes much more difficult. Decapping with fuming Nitric Acid gives little success—the coating simply turns to a goopy mess. The assembler can only rely on electrical testing and analysis. Ongoing reliability testing (ORT) via thermal cycling is a good tool to weed out weaknesses and improve the process.

Die level analysis may prove quite unsettling for a board assembler. Developing a close alliance with a capable laboratory specialized in this task and with the die supplier greatly helps. A COB problem could be a legitimate die problem or board assembly related. Take for instance the die defect shown in Figure 6. This classical case of electrical overstress

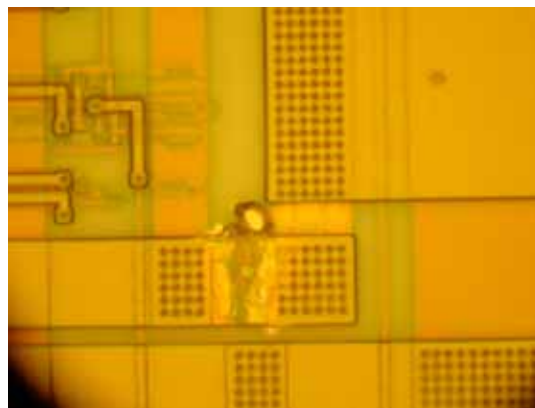


Figure 6. EOS die defect.

could manifest in similar ways from the assembly process or from a congenital weak spot in the die. It requires further detailed Scanning Electron Microscope (SEM) cross-section examination with close cooperation between the assembler and die supplier for root cause identification. The assistance of wafer fab engineers, related die lot defectivity count, die structure details such as number of metal layers, passivation and the type of process etc. provide vital clues for proper analysis. Without that cooperation the determination can lead down a rocky road with a lot of gray areas.

**Reworking COB**

As with any process rework must be considered. Some dies will inevitably fail and die selection may not always be optimal. COB rework is applied at three different levels listed below in descending order of success.

**Level 1: Bonds missing or mis-bonds:**

This is doable only if space around the die pad and board metallization permits bonding a new wire without disturbing adjacent bonds. Bonds must be on fresh areas and never over previous footprints. If space limits access, the die must be completely removed and the processes redone per item B below.

**Level 2: Die replacement before encapsulation:**

This is the case when a die is found damaged at VMI or defective during the testing prior to encapsulation. The first step is the removal of the bond wires by a sharp needle under magnification. Next, removal of the die requires controlled localized heating to achieve softening and breakdown of the die bond adhesive (typically around 200° C). Heating is mostly top-side convective but could be radiant. Critical factors are controlling maximum tempera-

tures and keeping gradients under 3 °C/sec to prevent degradation of any sensitive components. The defective die is easily pried off upon adhesive break down. After a visual for any site damage, remnants of the die-attach and bond wires are removed and the site cleaned thoroughly and re-inspected. The process then follows the prime sequence except new bonds must be on new areas and never over previous footprints.

### Level 3: Die replacement after encapsulation:

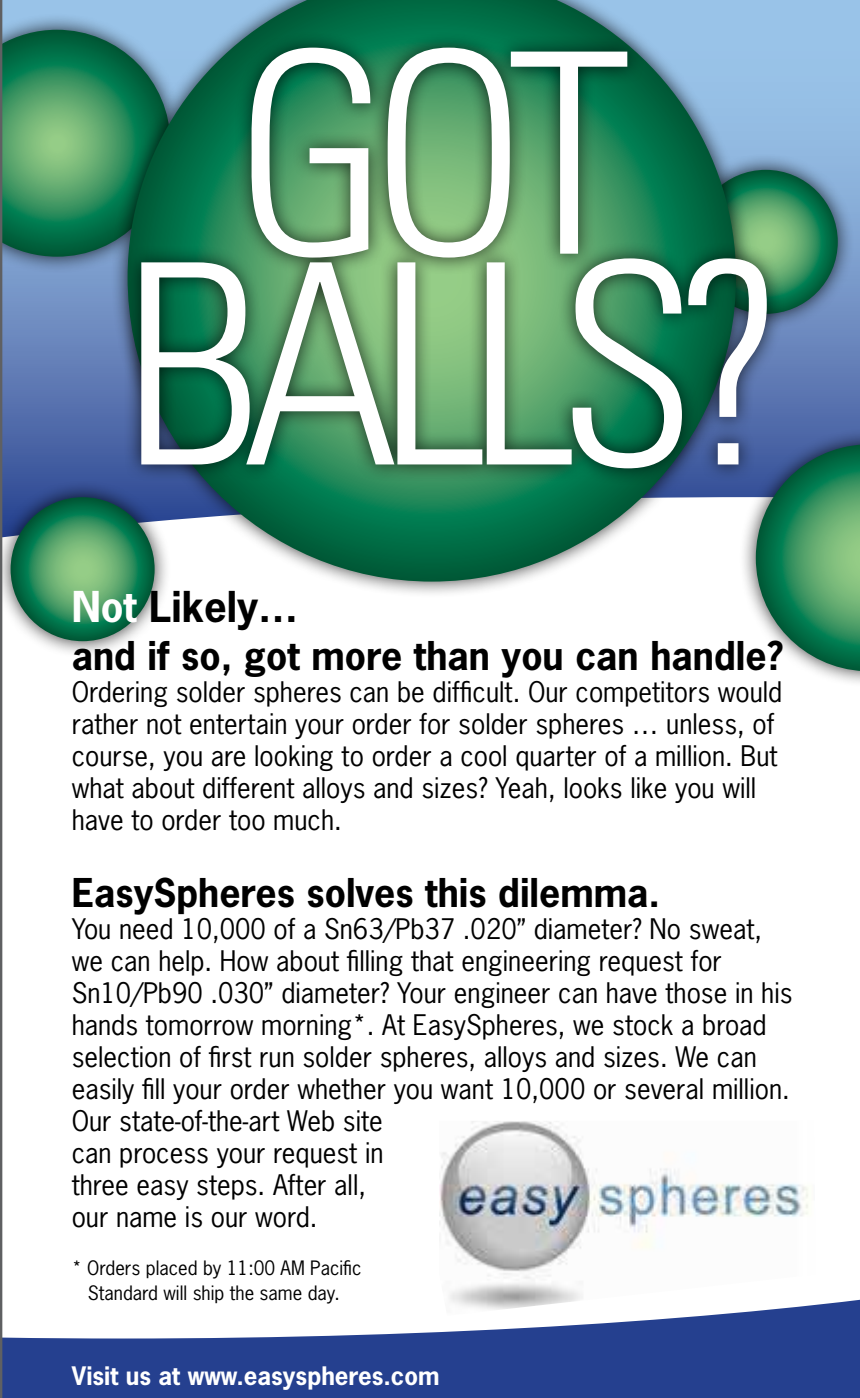
When a fully completed and encapsulated assembly fails final test and the fault traced to the COB, the defect could be either the die or bonding. Rework requires removing the encapsulation followed by the sequence of item B above. As with die removal, the encapsulation is softened to the point of degradation by topside convective heating. When it loses its bond to the base material it is then pried off. The steps then proceed along item B above. Level 3 is not encouraged; it is not pretty and has low probability of success.

Rework of COB may appear tedious but it is doable. Between Level 1 and Level 2 rework may help recover as much as 80% of defective assemblies. The process nature and pad width limit rework to one time.

### Summary & conclusion

COB is a viable process with many applications in relatively modest cost products with relatively short life cycle and where time to market and 'first-in-the-game' a key ingredient for success. Die cost, sizing, I/O, complexity, foundry maturity and UBD are key factors in selecting dies for COB. Successfully merging COB with surface mount processes requires understanding, controlling and managing a whole new set of complex variables related to the wire bonding process. A 10 K or better class clean room and associated discipline is highly recommended. Challenges for the board assembler lie in acquiring skills, knowledge and resources more attuned to IC back end processes and coupling them with SMT know how.

Top critical factors are a COB friendly PCB layout, die supplier management, bond reliability and a pre-encapsulation test regimen. Critical process control points are contamination control, tool management, and wire loop and encapsulation height control. Higher end applications and component manufacturing like BGA assembly require plasma etching or stripping. Although flip



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chips and flip chip CSPs (FCCSP) compete with COB, each has its own uniqueness and 'best-fit' market segments. COB is a mature process, using state of the art equipment, and is currently serving across a wide range of products and applications as a DCA alternative to IC packaging. COB has as its roots wire bonding, a technology with some four decades of development and maturity behind it.

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